an access circuit connected to the memory to access, during said access

sequence, all of the bits stored in <u>all of</u> said plane<u>s</u> of said memory

cells; and

an orthogonal error detection circuit connected to the access circuit and

said memory to detect an error in a bit accessed during said access

sequence, comprising:

a row error detection circuit to detect an error in a bit of a row of said

accessed bits;[and]

a column error detection circuit to detect an error in a bit of a column

of said accessed bits<u>; and</u>

<u>a stack error detection circuit to detect an error in a bit of a stack of</u>

<u>said accessed bits</u>.

Amend claim 15 as follows:

15. (Once amended) The memory system of claim 14 wherein said first<u>,</u>

<u>second</u> and [second]<u>third</u> error detection circuits also correct said bit errors,

respectively.

Cancel claim 16.

Amend claim 24 as follows:

24. (Once amended) A circuit for use in a memory system comprising:

a memory comprising a plurality of dynamic memory cells arranged in a

plane of <u>m</u> rows and <u>n</u> columns, each cell storing a bit;

an access circuit connected to the memory to access, during an access

[sequence]<u>cycle</u>, all of the bits stored in <u>a selected one of</u> said

[plane]<u>rows</u>; and

a row error detection circuit connected to the access circuit and said

memory to detect an error in a bit of <u>said</u> row of said accessed bits;

the circuit comprising:

a parity generation circuit connected to said memory to generate, during each access cycle in which any of said accessed bits are stored, [a]n parity bits, each related to all m bits stored in respective one of said columns.

Amend claim 31 as follows:

31. (Once amended) A random access error detection and correction (RAEDAC) unit for detecting and correcting errors in an ordered bit string of predetermined length, the RAEDAC comprising:

a parity generation circuit which receives, in any order, each bit of said string, and generates a plurality of parity bits, each related to a unique combination of said bits comprising said string;

a[n error detection] parity check circuit connected to said parity generation circuit to detect an error in a bit of said string using said parity bit; and

an error correction circuit coupled to the parity check circuit to correct said detected bit error.

Amend claim 32 as follows:

32. (Once amended) The RAEDAC of claim 31 wherein the [error detection]parity check circuit detects multi-bit errors in said string using said parity bits.

Add new claims 33, 34 and 35 as follows:

33. (New) A random access error detection and correction (RAEDAC) unit for detecting and correcting errors in an ordered bit string of predetermined length, the RAEDAC comprising:

an error correction code generation circuit which receives, in any order, each bit of said string, and generates a plurality of check bits, each related to a unique combination of said bits comprising said string; and

an error detection circuit connected to said error correction code generation circuit to detect an error in a bit of said string using said check bits.

34. (New) The RAEDAC of claim 33 further comprising:

an error correction circuit coupled to the error detection circuit to correct said detected bit error.

35. (New) The RAEDAC of claim 33 wherein the error detection circuit detects multi-bit errors in said string using said check bits.

Remarks

Claims 1-32 are pending in the present application for patent. In the Office Action of 27 September 2001 (the "Office Action"): claims 1-9, 14-15 and 19-32 were rejected under 35 U.S.C. § 103 as being obvious in view of Ozaki, *et al.*, US 4,719,628 ("Ozaki"), and claims 10-13 and 16-18 were objected as being dependent upon a rejected base claim. In response, Applicants have amended claims 14, 15, 24, 31 and 32, cancelled claim 16, and added new claims 33-35.

The Official Draftsman has objected to Figures 4 and 8B as having improper margins, and to Figure 9 as having lines through certain of the text labels. Further, in reviewing the specification and drawings in anticipation of allowance, Applicants noticed that the first and fourth rows of the table comprising Fig. 5A were improperly labeled, on the left side thereof, "SET" when, as described in lines 1-3 of page 17 of the specification, it is clear that such rows should have been labeled "CLEAR". In addition to making these corrections, Applicants have deleted the attorney docket number from the face of all Figures. Applicants have submitted herewith substitute copies of Figures 1 through 9, and respectfully request the Official Draftsman to enter these corrected drawings.

In view of these amendments, Applicants respectfully submit that the application is now in full compliance with all applicable formal requirements, and that claims 1-35 are patentable over the references of record for the reasons set forth below.

The Rejection under 35 USC 103(a):

In the Office Action, the Examiner has rejected claims 1-9 under 35 U.S.C. § 103 as being obvious in view of Ozaki. However, even after careful consideration, Applicants fail to understand the relevance of Ozaki. In particular, claims 1-5 are directed to the embodiment shown in Figure 1, while claims 6-9 are directed to the embodiment shown in Figure 2. In both